Analysis and Experimental Study of an L-band New Topology Doherty Amplifier

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***ABSTRACT* — This paper describes the first design of an L-band unbalanced-topology Doherty amplifier fabricated with FET devices. In the proposed topology and unlike the standard one, the carrier amplifier operates (at low input derive levels) into a load impedance three times larger than its optimum. Thus, theoretically the Doherty amplifier achieves 78.5 % of efficiency at 7.24-dB back-off. At 11-dB back-off from the maximum output power of 26.7 dBm, the measured Doherty amplifier power added efficiency achieves 35.2 % at 1.9 GHz that is 18.5 % higher than that of a Class B amplifier. Optimum values of Doherty amplifier load and quarter-wave transformer characteristic-impedance were determined. The theory and design of this amplifier with its new topology will be discussed.**

I. Introduction

The need for high-efficiency and linear microwave power amplifiers has grown rapidly, especially as mobile and satellite communication systems have been developed and expanded. These systems mandate that the amplifier efficiency be as high as possible in order to extend the operating time of portable power sources. For acceptable linearity in handling multi-carrier signals, output power must be backed off from its peak value. Thus, the amplifier efficiency is reduced from its maximum by the amount of back-off. Such trade-off between linearity and efficiency was difficult to solve with conventional amplifiers. Fortunately in a Doherty amplifier, the efficiency can be maintained high at certain amount of the output power back-off. Previous realizations of the Doherty amplifier with promising results at L-band and Ku-band were reported in [1]-[4]. These realizations dealt only with the standard topology of this amplifier that theoretically achieves an efficiency of 78.5% at 6-dB back-off from its maximum output power. In the reported conventional topology and at low derive levels, the carrier amplifier operates in a load two times larger than its optimum. At maximum derive level, the load apparent to both carrier and peak amplifiers is the optimum load. Thus, in this topology the carrier amplifier turns on when the input signal reaches half of its peak value.

In this paper, we report a first demonstration of a Doherty amplifier with a new topology that theoretically achieves an efficiency of 78.5 % at 7.24-dB back-off from its maximum output power. In this topology, the carrier amplifier turns on before the input signal reaches half its peak value. Thus, the peak amplifier used in the proposed topology is biased more near the pinch-off than that used in the standard topology. This has the advantage of avoiding the gate-breakdown phenomena that could happen in the peak amplifier.

II. Basic Principle Of The Doherty Amplifier New Topology

A simplified block diagram of a two-stage Doherty amplifier is shown in Figure 1. Amplifier 1 is referred to as the carrier amplifier and is operated as Class B. Amplifier 2 is referred to as the peak amplifier and is operated as Class C, it turns on when the carrier amplifier starts to compress. A quadrature 3-dB hybrid is used at the input of the circuit. The output power from the two amplifiers is combined with a quarter-wave impedance transformer. Thus, the output signals of the two amplifiers will combine in phase.

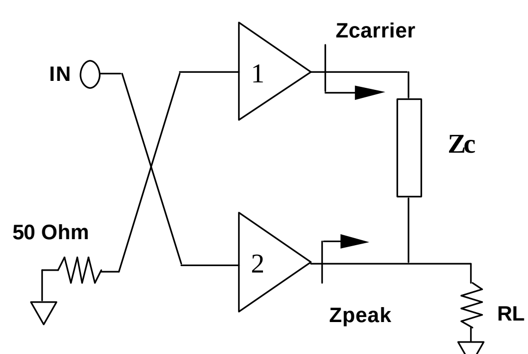

Fig. 1. Doherty amplifier topology.

The characteristic impedance of the quarter-wave transformer is defined as:

$$Z_c = \sqrt{3 \cdot R_{opt} \cdot R_L} \qquad (1)$$

Where R_L is the actual load of the Doherty amplifier and R_{opt} is the optimum load of the carrier and peak amplifiers.

Following analysis given in [5], characteristics of the Doherty amplifier in its new topology can be determined. At low input derive levels the peak amplifier is off and delivers no power to the load. As the input derive increases the carrier amplifier, loaded with $3R_{opt}$, begins to saturate and reaches its maximum efficiency at an input derive power level lower than would be the case for a $2R_{opt}$ load.

At these input derive levels, the maximum output power and efficiency of the Doherty amplifier are given by:

$$P_L = \frac{1}{24} \cdot \frac{V_{d\max}^2}{R_{opt}}, \qquad (2)$$

$$\eta = \frac{\pi}{4} \qquad (3)$$

Where V_{dmax} is the maximum drain voltage of the carrier and peak amplifiers.

At medium input derive levels and as the power delivered by the peak amplifier increases, the load presented to the carrier amplifier decreases but will not approaches R_{opt} as the case in the standard topology of the Doherty amplifier. The output power of the Doherty amplifier is given by:

$$P_M = \frac{1}{2} \cdot \frac{V_{out}^2}{R_L} \qquad (4)$$

Where V_{out} is the Doherty amplifier output voltage.

At high input derive level, the peak amplifier, presented with R_{opt} load, will deliver more power to the Doherty load than the carrier amplifier presented with a load higher than R_{opt} but lower than $3R_{opt}$. This is because in the proposed topology the peak amplifier turns on before the input signal reaches half its peak value (unlike the standard topology). At this stage of input derive levels, the maximum output power, voltage, and efficiency of the Doherty amplifier are given by:

$$P_H = \frac{1}{8} \cdot \frac{V_{d\max}^2}{R_L}, \qquad (5)$$

$$V_{out} = \frac{V_{d\max}}{2}, \qquad (6)$$

$$\eta = \frac{\pi}{4} \qquad (7)$$

The optimum values of the Doherty amplifier load and quarter-wave transformer impedance that should be used in the proposed topology are given by:

$$R_L = 0.566\, R_{opt}, \qquad (8)$$

$$Z_c = \sqrt{1.7}\, R_{opt} \qquad (9)$$

Now knowing the value of the Doherty amplifier load, one can calculate that maximum output power back-off insuring a near peak of efficiency using (2) and (5):

$$Back\!-\!off = 10\,Log\left(\frac{P_H}{P_L}\right) = 7.24\,dB \qquad (10)$$

The behavior of the instantaneous efficiency of a typical class B amplifier and instantaneous efficiency of the proposed Doherty amplifier topology versus the normalized output voltage are shown in Figure 2. This Figure illustrates that throughout 7.24 dB output power back-off the overall amplifying efficiency remains near the maximum attainable linear efficiency.

III. Circuit Design And Experimental Results

In order to investigate the performances and merits of the proposed topology, a Doherty amplifier was designed at central frequency 1.9 GHz using HP-MDS. The carrier and peak amplifiers were designed using Fujitsu FLL107ME transistors on duroid substrate, $\varepsilon_r = 2.33$, h = 20 mils. During operation of the amplifier the carrier device is biased near pinch-off for Class B (Vgs = -2.08 V) while the peak device is biased below pinch-off for Class C (Vgs = -2.73 V). A standard broadband branch-line coupler was used as the quadrature input hybrid network. The isolated port was terminated with external 50-Ohm resistor. This coupler is useful for achieving a low-input VSWR for the amplifier. The 50-Ohm load impedance is transformed to the desired optimum load with a matching network at the output of the circuit. For comparison purposes, a Class B amplifier (biased at Vgs

= -2.1 V) was also designed on the same substrate. Both Doherty amplifier and class B amplifier were tested at room temperature. The measured output power under one tone excitation for Doherty amplifier is shown in Figure 3. This Figure shows also the power added efficiency of the Doherty amplifier and class B amplifier. At 11-dB back-off from the maximum output power, the Doherty amplifier achieves 35.2 % of power added efficiency that is 18.5 % higher than that of a Class B amplifier. The measured Doherty amplifier gain, output efficiency, and class B output efficiency are shown in Figure 4.

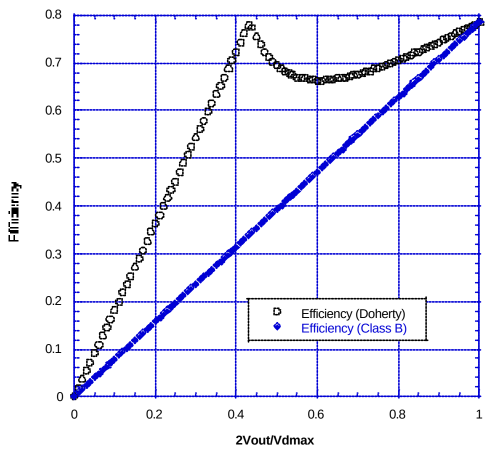

Fig. 2. Theoretical instantaneous efficiency of the Doherty amplifier (proposed topology).

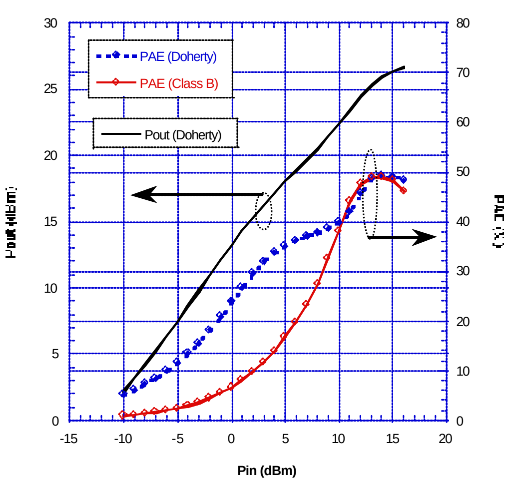

Fig. 3. Measured Doherty amplifier power added efficiency (PAE) and output power, and Class B amplifier power added efficiency.

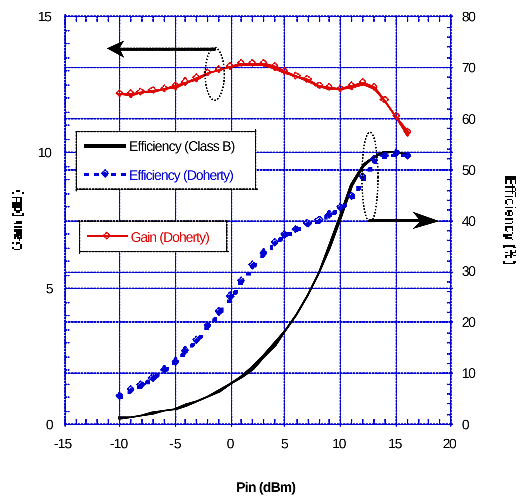

Fig. 4. Measured Doherty amplifier efficiency and gain, and Class B amplifier efficiency.

IV. CONCLUSION

This work describes the first demonstration of a new topology Doherty amplifier fabricated with FET devices. When compared to the standard topology, the new one has mainly two advantages: it insure a high efficiency at more output power back-off. The peak amplifier is biased more near the pinch-off thus avoiding the gate-breakdown phenomena. The measured overall efficiency of the Doherty amplifier remains higher than 35 % when the output power is backed-off of 10-dB from its maximum value. This is a very attractive feature especially for amplifying multi-carrier signals.

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